In regard to the objections to the drawings, a Request for Approval of Drawing Changes accompanies this Amendment to change the drawings as required by the Examiner. Specifically, a new FIG. 3 has been added to illustrate the differential sinusoidal signal pair. No new matter has been added, inasmuch as FIG. 3 is fully supported by the disclosure in paragraph 18 of the specification.

Also, in regard to FIG. 1, the clock splitters 36 are now shown to split the local clock.

All of the pending claims were rejected as either being anticipated by or obvious in view of the Wissell et al. reference.

Claim 1 is directed to a "method of generating a clock signal on an integrated circuit (IC)", including the steps of "generating a differential sinusoidal signal pair" and "generating a clock signal from the differential pair for the IC".

Applicants wish to respectfully direct the Examiner's attention to paragraph 18 of the specification, at which the term "differential sinusoidal signal pair" is defined as "a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180° out of phase with each other" (Emphasis added). It is noted that this definition is consistent with the conventional understanding of the term "differential sinusoidal signal pair".

Applicants note that generation of a differential sinusoidal signal pair, as so defined, and generation of a clock signal therefrom, are not disclosed or suggested by the Wissell et al. reference. In the portion of its disclosure that is most nearly relevant to the present invention, the Wissell et al. reference discloses, at column

5, lines 6-10, "a phase splitter 42...for producing clock signals at phases that are 90° apart, i.e. quadrature-related clock signals". Thus the plural clock signals generated in Wissell et al. are 90° apart, not 180° apart, as is the case of the claimed differential sinusoidal signal pair. In other words, quadrature related clock signals, as disclosed in Wissell et al. are different from a "differential sinusoidal signal pair" as recited in claim 1 and defined in the specification. Accordingly, the Wissell et al. reference fails to teach or suggest the invention as specifically recited in claim 1. It is therefore submitted that the rejection of claim 1 based on the Wissell et al. reference should be reconsidered and withdrawn.

Claim 8, which is the next independent claim, recites "distributing a clock signal in the form of a differential sinusoidal signal pair" in a portion of a clock tree of an IC. As pointed out above, Wissell et al. fails to disclose a differential sinusoidal signal pair. Accordingly, claim 8 is submitted as patentable on the same basis as claim 1.

The next independent claim, which is claim 13, recites "a generating circuit adapted to generate a differential sinusoidal signal pair". It will be appreciated that claim 13 is submitted as patentable on the same basis as claim 1, since the Wissell et al. reference fails to disclose a differential sinusoidal signal pair. Note that any amendment made to claim 13 (1) has been made solely for clarification purposes; (2) is not intended to narrow the scope of claim 13; and (3) is not being made for any reason which relates to the statutory requirements for a patent.

Claim 22, which is the next and final independent claim, recites "means for generating a differential sinusoidal signal pair", and is accordingly submitted as patentable on the same basis as the other independent claims.

The claims which have not been explicitly referred to above are all dependent claims, and are submitted as patentable on at least the same basis as their respective parent independent claims.

For the foregoing reasons, it is submitted that all of the claims are in condition for allowance, and passage to issue is respectfully solicited.

Applicants do not believe any fees are due regarding this amendment. If any fees are required, however, please charge Deposit Account No. 04-1696. Applicants encourage the Examiner to telephone Applicants' attorney to discuss the amendment should any issues remain.

Respectfully submitted,

Brian M. Dugan, Esq.
Registration No. 41,720
Dugan & Dugan, LLP
Attorneys for Applicants
(914) 332-9081

Dated: March 7, 2002
Tarrytown, New York

VERSION MARKED TO SHOW CHANGES

In the Specification:

Paragraph 14 has been amended as follows:

FIG. 1 is a schematic block diagram representation of a clock signal generation and distribution arrangement provided in accordance with the invention; [and]

Paragraph 15 has been amended as follows:

FIG. 2 is a schematic diagram of a typical one of the clock receivers shown in FIG. 1[.]; and

Paragraph 18 has been amended as follows:

In FIG. 1, reference numeral 10 indicates a signal generator which generates a differential sinusoidal signal pair. As is well understood by those who are skilled in the art, a differential sinusoidal signal pair comprises a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180° out of phase with each other, as illustrated in FIG. 3. The differential sinusoidal signal pair generated by signal generator 10 may, for example, have a peak to peak differential (ppD) of about 100 mV or 150 mV. The common mode level of the differential sinusoidal signal pair may be at the center of the power supply voltage. For example, each signal of the pair may swing from about 575 mV to 625 mV when a 1.2 volt power supply is used. It will be recognized that such a differential sinusoidal signal pair has a peak to peak differential of 100 mV. It is contemplated to employ a differential sinusoidal signal pair having a different common mode and/or a different peak to

peak differential than the signals which have been described above.

Paragraph 23 has been amended as follows:

It may be desirable for [that] the distribution circuitry 12 to be routed and loaded so as to have inductance and capacitance that produces resonance at the desired frequency of operation. This further reduces the clock power requirements. Switchable loads 14 may be included in the distribution circuitry 12 to permit the load of the distribution circuitry 12 to be tuned to compensate for manufacturing variations.

In the Claims:

Claim 13 has been amended as follows:

13. (Amended) A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal signal pair;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals.